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Art Unit: 2419

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 7-12 and 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Abiru et al. (US 2003/0053481 A1).

Regarding claim 1, Abiru discloses an IPv6 header receiving apparatus (Fig. 1, 100) comprising:

a register (70) with a data size that is multiple of and octet, which receives IPv6 header data in units of an octet, stores the IPv6 header data, and transmits the stored IPv6 header data to an IPv6 processing module (30, 20) that corresponds to the IPv6 header data (0077; 0080; 0140-0142; 0232); and

modules for an IPv6 basic header or various types of IPv6 extended headers, which receive the IPv6 header data from the register and process the IPv6 header data (0233).

Regarding claim 2, Abiru discloses an IPv6 header receiving apparatus comprising: a counter which counts up to a specified amount of IPv6 extended header data that is transmittable in units of an octet at a time (0142);

a register with a data size that is a multiple of an octet, which receives IPv6 header data in units of an octet, stores the IPv6 header data, and, if the counter has completed counting up to the specified amount, transmits the stored IPv6 header data to a module for processing an IPv6 header that corresponds to the IPv6 header data (0077; 0080; 0140-0142; 0232); and

modules for an IPv6 basic header or various types of IPv6 extended headers, which receive the IPv6 header data from the register and process the IPv6 header data (0233).

Regarding claim 3, Abiru discloses an IPv6 header receiving apparatus comprising:

an octet indicator which counts up to an amount of IPv6 extended header data that can be transmitted in units of an octet at a time;

a register (70) with a data size that is a multiple of an octet, which receives IPv6 header data in units of 8 octets and stores the IPv6 header data (0140);

a control unit (30, 20), which analyzes the IPv6 header data stored in the register to determine a type and length corresponding to the IPv6 header data, and, if the octet indicator has completed counting up to the specified amount, instructs the register to transmit the IPv6 header data with the determined length to an IP header processing module that corresponds to the IPv6 header type (0077; 0080; 0140-0142; 0232); and

modules for an IPv6 basic header or various types of IPv6 extended headers, which receive the IPv6 header data from the register and process the IPv6 header data (0233).

Regarding claim 4, Abiru discloses wherein the register comprises:

a temporary register with a data size that is a multiple of an octet, which receives IPv6 header data in units of an octet and stores the IPv6 header data; and

a shift register, which receives the IPv6 header data in units of an octet each time from the temporary register and, if the shift register is filled with an amount of data to be transmitted at one time to a module, the shift register transmits the filled amount of data to the modules (0192-0194).

Regarding claim 7, Abiru discloses wherein the modules are a basic header module, a routing header module, a destination option header module, an authentication header module, an ESP header module, a hop-by-hop header module, and an upper layer module (0005; 0055; 0168).

Regarding claim 8, Abiru discloses an IPv6 processing method comprising:

Filling a register with IPv6 header received in units of a predetermined size, which is a multiple of an octet; (0077)

Identifying an IPv6 header type by analyzing the IPv6 header data filled in the register (0065-0066; 0234); and

Transmitting the IPv6 header data to a module corresponding to the identified IPv6 header type (0066; 0234).

Regarding claim 9, Abiru discloses and IPv6 header processor comprising: a data link layer, which transmits data transmissions (0065);

an IPv6 controller (30), which is responsive to header data of the data transmissions from the data link layer; and detects a type and length of the header data, and outputs the header data based on the type and length of the header data detected in the data transmissions (0065;0077; 0080) and

a register file having a plurality of IPv6 header modules, coupled to the IPv6 controller, each IPv6 header module receives and processes the corresponding header data transmitted by the IPv6 controller (0086-00883).

Regarding claim 10, Abiru discloses wherein the IPv6 controller comprises:

storage registers (70) to store the header data of data transmissions (0140);

a counter (10) which increments a value of an indicator when an octet of the header data is received (0032; 0142); and

a control unit which detects the type and length of the header data, and outputs the header data from the storage registers based on the indicator value, to the corresponding IPv6 header module, wherein the corresponding IPv6 header module is determined based on the detected type and length of the header data, wherein the corresponding IPv6 header module processes the header data (0140-0142; 0232-0233).

Regarding claim 11, Abiru discloses wherein the storage registers and the plurality of header processors are each multiples of and octet (0232).

Regarding claim 12, Abiru discloses wherein the storage registers comprise: a buffer register to receive data transmissions in multiples of and octet (0140; 0232); and

a transmit register, wherein the buffer register outputs octets of header data to the transmit register where the header data is stored, and when the indicator value is equivalent to a predetermined value the contents of the transmit register are output under direction of the control unit (0080).

Regarding claim 14, Abiru discloses a method of processing header data comprising: shifting header data into a first register (60) in packets of lengths that are multiples of an octet (0021; 0140);

transmitting the header data into a second register (70) where the header data is maintained (0021; 0140);

determining a type and length of the header data, which determines the output path of the header data maintained in the second register (input unit 60 detects the arrival of receiving packet and synchronizes the receiving packet with a clock from the head of the packet to be sequentially and directly stored in register 70);

incrementing a counter each time the header data is transmitted to the second register from the first register (packet length signal 223 (which is measured and obtained at the packet data input unit 60) is held until new packet data re outputted to the packet data holder 70); and

shifting the contents of the second register to a predetermined processing module by the determined output path when the counter reaches a predetermined value (0021-0023; 0032; 0167-0169).

Regarding claim 15, Abiru discloses wherein the header data is in IPv6 format (0166).

Regarding claim 16, Abiru discloses further comprising counting a maximum effective length of each header data (0142); and

determining whether the maximum effective length of each header data exceeded a predetermined value, wherein if the predetermined value is exceeded a next header data packet is received (0228; 0284).

Regarding claim 17, Abiru discloses wherein if the predetermined value is not exceeded additional header data is shifted into the first register (0284).

Regarding claim 18, Abiru discloses further comprising receiving the header data from a media access control layer (0004).

Allowable Subject Matter

3. Claims 5, 6 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Paatel et al. (US 2006/0209840 A1) discloses a system and method for providing transformation of multi-protocol packets in a data stream.

Dyckerhoff et al. (US 6,976,154 B1) disclose pipelined processor for examining packet header information.

Larson et al. (US 4,418,382) discloses information exchange processor.

Brender et al. (US 3,638,195) discloses digital communication interface.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SABA TSEGAYE whose telephone number is (571)272-3091. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on (571) 272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wing F. Chan/ Supervisory Patent Examiner, Art Unit 2619 10/7/08 Saba Tsegaye Examiner Art Unit 2419

/S. T./ Examiner, Art Unit 2419